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Skills

- Expertise in cache coherence in distributed shared-memory multiprocessors. Long experience with SCI cache coherence.
- Experience in designing, simulating and documenting multiprocessor memory systems with an emphasis on cache coherence protocols.

Research Interests

Computer Architecture. Memory systems. High-performance shared-memory architectures. Cache coherence. Instruction-based optimizations for shared-memory. Processor-memory integration.

Education

- University of Wisconsin-Madison. Ph.D. in Computer Science (Computer Architecture), in progress. Expected graduation date: August 1998.

  Advisor: James R. Goodman. Thesis: <u>Static, Dynamic, Address-based and Instruction-based Optimizations for High-Performance, Scalable Shared-Memory.</u>

  Ph.D. Minor in Business (grad. courses in Marketing & Administration)
- University of Wisconsin-Madison. M.S. in Computer Science, May 1993.
- National Technical University of Athens. B.S. in Electrical & Computer Engineering, June 1991.

Contributions of my work

- Proposed **Instruction-based Prediction** to optimize sharing patterns (migratory sharing, wide sharing, and producer-consumer sharing) in distributed shared-memory multiprocessors. (Thesis topic)
- Proposed **GLOW**, a comprehensive solution for handling widely shared data in distributed shared-memory multiprocessors. (Thesis topic)
- Proposed the **Distributed Vector Architecture** (DIVA) that executes vector programs on a collection of highly integrated processor/memory nodes. DIVA minimizes inter-node communication using dynamic computation mapping. Joint work with Rabin Sugumar and James Schwarzmeier.
- Proposed the **DataScalar Architecture** that improves memory system performance for unmodified serial applications by executing computation redundantly across multiple highly integrated processor/memory nodes. Joint work with Douglas C. Burger and James R. Goodman.

Work experience

- **Internship, CRAY Research Inc.**, Summer 1996. Developed fundamental concepts for novel Distributed Vector Architectures and high-performance computing based on integrated processor-memory nodes.
- **Research Assistant** University of Wisconsin-Madison 1993-present.
- **Teaching Assistant**

  University of Wisconsin, 1991-1993. UNIX and programming consultant. Assisted in teaching graduate-level computer architecture course and introductory programming courses.

  National Technical University of Athens 1989-1991. Assisted in teaching Compilers course and consulted in the Digital Computers Lab.

Publications

Standards

[1] Stefanos Kaxiras. "IEEE Standard for Cache Optimization for Large Numbers of Processors Using the Scalable Coherent Interface 1596.2-1997"

Conference Papers

[2] Stefanos Kaxiras, Stein Gjessing, and James R. Goodman. "A Study of Three Dynamic Approaches to Handle Widely Shared Data in Shared-Memory Multiprocessors." To appear in *Proceedings of the International Conference on Supercomputing, July 1998*.

[3] Stefanos Kaxiras and James R. Goodman. "Improving Request-Combining for Widely Shared Data in Shared-Memory Multiprocessors." In *Proceedings of the Third International Conference on Massively Parallel Computing Systems (MPCS), April 1998.*

[4] Doug Burger, Stefanos Kaxiras, James R. Goodman. "Datascalar Architectures." In *Proceedings of the 24th Annual International Symposium on Computer Architecture*, June 1997.

[5] Stefanos Kaxiras and James R. Goodman "The GLOW Cache Coherence Protocol Extensions for Widely Shared Data." In *Proceedings of the International Conference on Supercomputing*, May 1996. Extended version*: University of Wisconsin-Madison CS Dept. TR-1305*, March 1996

[6] Stefanos Kaxiras "Kiloprocessor Extensions to SCI." In *Proceedings of the 10th International Parallel Processing Symposium*, April 1996.

Journal Papers

[7] Stefanos Kaxiras, Doug Burger, James R. Goodman. "A Memory-Centric Approach to Computing: DataScalar." To appear in the *Journal of Systems Architecture*, *Special Issue on Microprocessor Architecture.*

[8] Antreas Stafylopatis, Ioannis Papakonstantinou, Stefanos Kaxiras. "PSM: Software Tool for Simulating, Prototyping, and Monitoring of Multiprocessor Systems." *Information and Software Technology* 34, May, 1992, pp. 313-325.

[9] Panagiotis Tsanakas, George Papakonstantinou, Stefanos Kaxiras. "A Hardware Synthesis Methodology Using Prolog." *Microprocessing and Micro-programming* 32 (1991) 307-314, North-Holland.

Workshop Papers

[10] Stefanos Kaxiras and Stein Gjessing. "Dynamic GLOW: Dynamic Optimizations for Efficient Large Scale Sharing." *8th International Workshop on SCI-based High-Performance Low-Cost Computing (SCIzzL 8)*, December 1997. Also as *University of Wisconsin-Madison CS TR-1351,* Dec. 1997.

[11] Stefanos Kaxiras, Rabin Sugumar, James Schwarzmeier. "Distributed Vector Architectures: Beyond a Single Vector-IRAM." *24th ISCA Workshop on Processor-Memory Integration: Chips that Compute and Remember*, June 1997. Earlier version: *University of Wisconsin-Madison CS Dept. TR-1339*, February 1997. Also available from CRAY Research.

[12] Stefanos Kaxiras and James R. Goodman. "Tools for SCI research in the University of Wisconsin." *3rd International Workshop on SCI-based High-Performance Low-Cost Computing (SCIzzL 3)*, August 1995.

[13] Stefanos Kaxiras and James R. Goodman. "Implementation and Performance of the GLOW Kiloprocessor Extensions to SCI on the Wisconsin Wind Tunnel." *2nd International Workshop on SCI-based High-Performance Low-Cost Computing (SCIzzL 2)*, March 1995.

[14] Stefanos Kaxiras and James R. Goodman. "Hierarchical Extensions to Cache Coherence in SCI." *1st International Workshop on SCI-based High-Performance Low-Cost Computing (SCIzzL 1)*, August 1994. Also as *University of Wisconsin-Madison CS Dept. TR-1235*, July 1994.

Technical Reports

[15] Stefanos Kaxiras. "The Use of Instruction-Based Prediction in Hardware Shared-Memory." *University of Wisconsin-Madison Computer Sciences Dept. TR-1368,* April 1998.

[16] Doug Burger, Stefanos Kaxiras, James R. Goodman. "DataScalar Architectures and the SPSD Execution Model." *University of Wisconsin-Madison CS Dept. TR-1317*, July 1996.

Other

[17] Stefanos Kaxiras, Rabin Sugumar, James Schwarzmeier. "Distributed Vector Architecture."

[18] Stefanos Kaxiras and James R. Goodman. "Improving CC-NUMA Performance Using Instruction-Based Prediction"

Patents

[1] **Distributed Vector Architecture**. Inventors: Stefanos Kaxiras, Rabin Sugumar. Application filed by CRAY Research/Silicon Graphics.

[2] **Interleaving Memory in Distributed Vector Architecture Multiprocessor Systems**. Inventors: Stefanos Kaxiras and Rabin Sugumar. Application filed by CRAY Research/Silicon Graphics.

[3] **Multiple Processor, Distributed Memory Computer with Out-of-Order Processing**. Inventors: Douglas C. Burger, Stefanos Kaxiras, James R. Goodman. Application filed by the Wisconsin Alumni Research Foundation.

Conference, Workshop and Invited Talks

- ISCA Workshop on Processor-Memory Integration, June 1997.
- Invited talk University of California-Berkeley, March 1997.
- Invited talk CRAY Research, March 1997.
- International Conference on Supercomputing, June 1996.
- International Parallel Processing Symposium, April 1996.
- SCIzzl 1 Aug. 1994, SCIzzl 2 Mar. 1995, SCIzzl 3 Aug. 1995.

Other Work

- Implemented the Linda parallel programming language in a network of workstations on top of the PVM message passing system and in the CM-5 parallel supercomputer.
- Implemented an original system for the automated synthesis of hardware using specifications in Prolog (B.S. Diploma Thesis).

Honors

Research Award, Apple Computer Inc., Summer 1995. Topic: GLOW Kiloprocessor Extensions to Scalable Coherent Interface (IEEE Std. 1596, 1992) now part of the IEEE proposed standard P1596.2.

Professional Activities

- **Editor, IEEE P1596.2**, “Standard for Cache Optimization for Large Numbers of Processors Using the Scalable Coherent Interface.” Responsible to edit and update the draft standard, and deliver its detailed specifications.
- Contributed to the development of IEEE 1596 related standards.
- Member IEEE Computer Society, ACM.
- Reviewer for ASPLOS 98, IEEE Trans. on Computers Dec. 98, ISCA ‘98, Computer ‘97, HIPC ‘97, ICPP ‘97, ICS ‘96.

Personal Information

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References

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