Techniques for Reducing Overhead of Shared-Memory Multiprocessing

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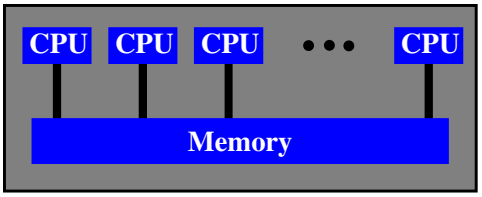
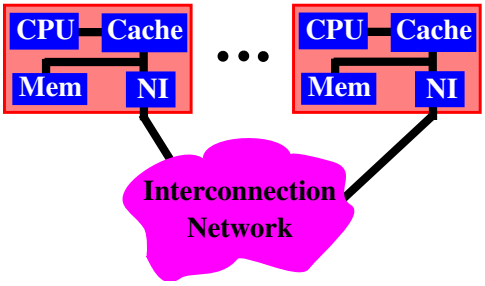
Shared-Memory Multiprocessing

Programming model



+ **uniform global address space**
+ **transparent communication**
+ **ease of programming**
+ **fine-grain communication**

Implementation



–but–

– **substantial overhead**

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Goal & Outline

Three opportunities to reduce overhead

- **Synchronization**
- **Memory model**
- **Data sharing patterns**

Outline

- **Scalable Coherent Interface**
- **Three classes of optimizations**
- **Experiments/methodology**
- **Evaluation**
- **Summary**

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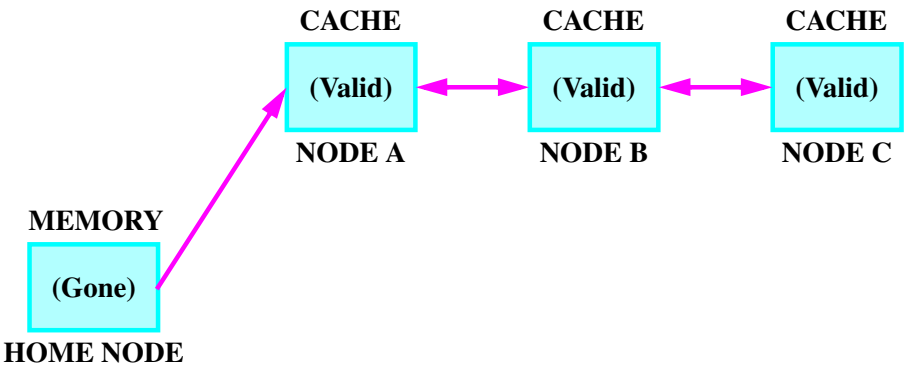
Scalable Coherent Interface (SCI)

- **Shared memory in hardware**
- **Complete specification (IEEE standard)**
- **Distributed, directory-based cache-coherence protocol**



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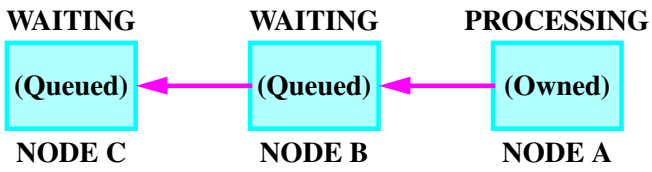
Synchronization Overhead

- **QOLB [ASPLOS III, 1989]**
  - **Hardware queue**
  - **+ reduced network traffic**
  - **+ reduced lock handoff latency**
  - **+ can couple lock & data**
  - **+ prefetch**
  - **– hardware implementation cost**



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Synchronization Overhead (cont'd)

- **MCS [ASPLOS IV, 1991]**
  - **QOLB-inspired software solution**
  - **+ no hardware required**
  - **+ reduced network traffic**
  - **– can't couple lock & data**
  - **– can't prefetch**

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Memory Consistency Overhead

- Sequential consistency
  - + intuitive
  - – overly restrictive
- Release consistency
  - + operations complete out of order
  - – programming complexity
  - – hardware support
- We study
  - Sequential consistency (seq)
  - 2 implementations of release consistency (r1, r2)

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Pairwise Sharing

- Optimize specific sharing patterns
  - No protocol is perfect
  - Extend for common patterns
  - 2-node sharing can be common
  - Pairwise sharing
    - Extend SCI for 2-node sharing

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Methodology

- **Wisconsin Wind Tunnel (WWT)**
  - **Discrete-event simulator on CM-5**
  - **Directly execute parallel shared-memory programs**
- **Benchmarks**
  - **Barnes, Mp3d, Ocean, Pthor, Water**
  - **Optimized for each experiment**

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Methodology (cont'd)

- **Simulation parameters:**
  - **Target system**

    32 processors, 1MB caches,

    4-way assoc., 64 byte cache line
  - **Non-blocking stores (write queue)**
  - **Validated constant network latency**

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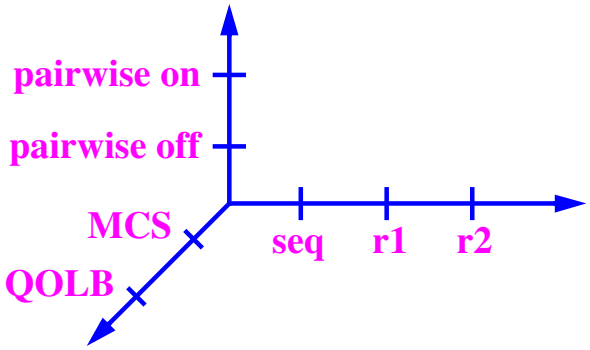
Experiments

- **Full cross product**



- **Base case: MCS, seq, pairwise off**
- **Future technology effects**

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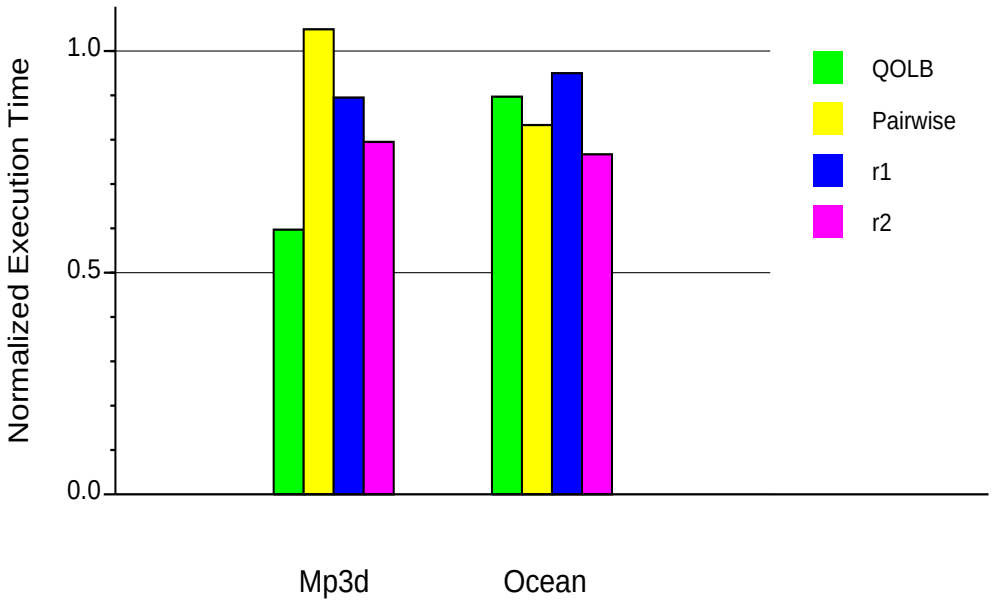
Experimental Results for Current Technology



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Optimization Interaction

Interaction	Benchmark	
	Mp3d	Ocean
Q+P	104%	106%
Q+r1	78%	93%
Q+r2	59%	88%
P+r1	97%	95%
P+r2	99%	57%

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Summary

- **Synchronization**
  - **QOLB very effective**
- **Memory model**
  - **r1 moderately effective and cheap**
  - **r2 very effective but expensive**
- **Pairwise sharing**
  - **Extremely good if 2-node sharing**
- **Future technology**
  - **Same trends, more dramatic speedups**

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Future Work

- **Breakdown of QOLB**
- **Scalability**
- **Percentage of overhead**
- **QOLB prefetch**

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Cache Size Issue

- **Problem**
  - **Benchmarks don’t strain large caches**
  - **Does this qualitatively affect results?**
- **Solution**
  - **Simulate very small (8K) cache**
  - **Compare optimization effects**
  - **Only pairwise sharing changed**

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Techniques for Reducing Overhead of Shared-Memory Multiprocessing
Backup

Optimization Interaction

Interaction	Benchmark	
	Mp3d	Ocean
Q+P	104%	109%
Q+r1	16%	86%
Q+r2	19%	74%
P+r1	97%	82%
P+r2	99%	40%

0.0% := no interaction

100.0% := additive

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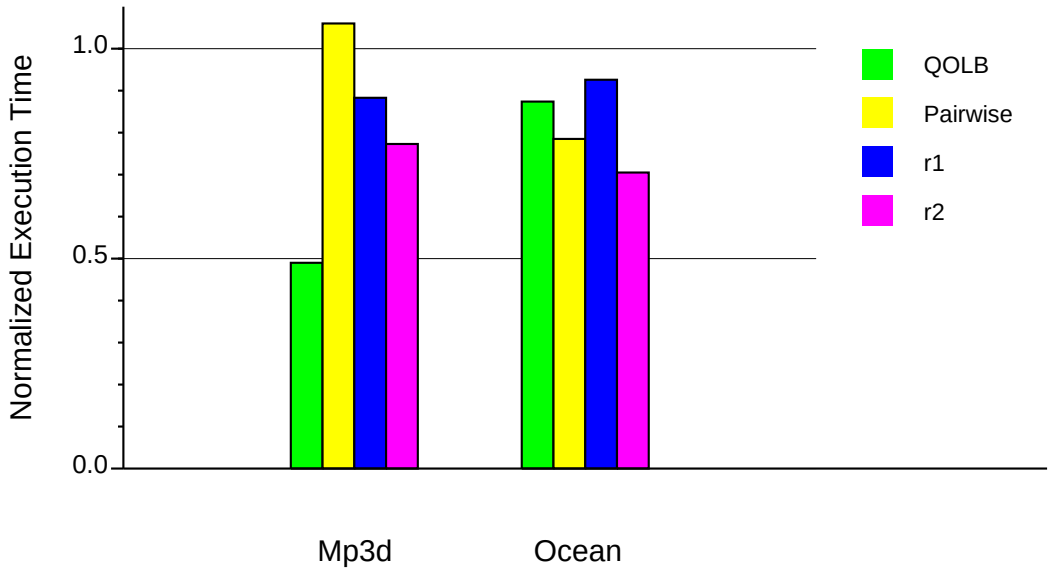
Experimental Results for Future Technology



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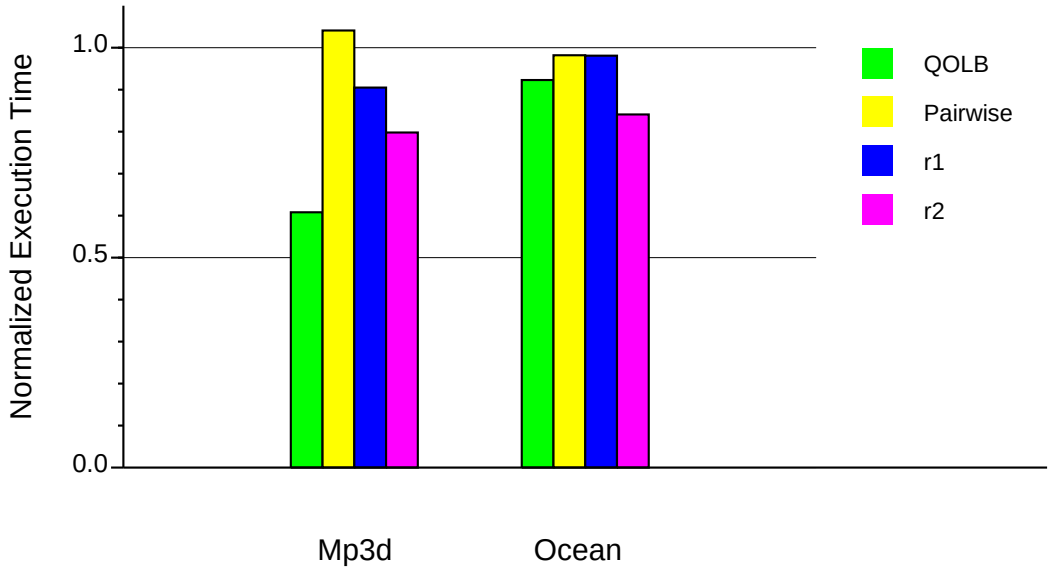
Experimental Results for Small Cache



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