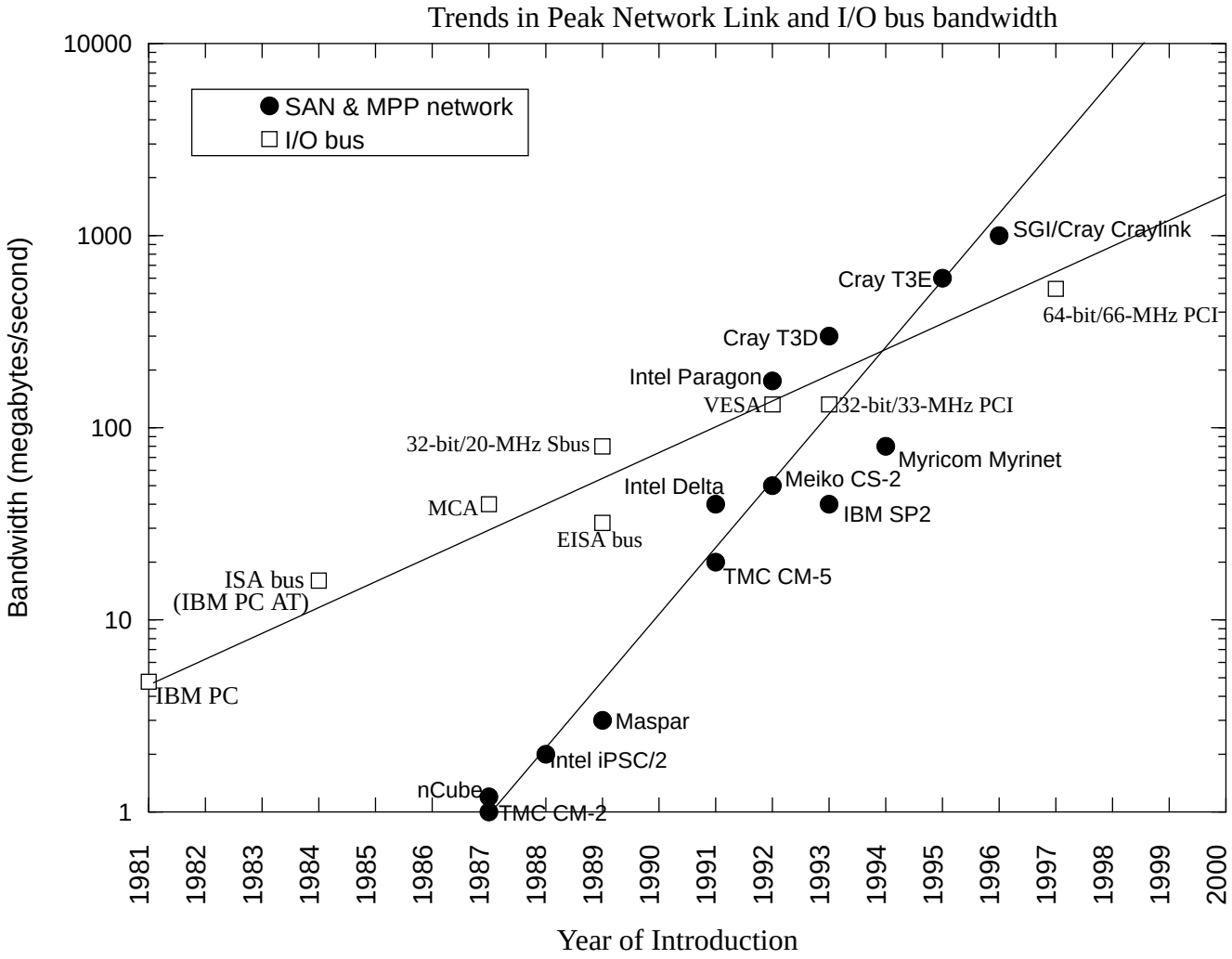

This figure shows the crossover point between peak System Area Network (SAN) and MPP network link bandwidths and “standard” I/O bus bandwidth. SAN and MPP link bandwidths have been increasing by roughly 100% per year, while the I/O bus bandwidth has been increasing by roughly 32% per year.

SAN and MPP network references: Cray T3E from Scott and Thorson, Hot Interconnects IV, 1996, and http://www.cray.com/news/9511/scalable.html, SGI Craylink from Galles, Hot Interconnects IV, 1996 and http://www.sgi.com/Headlines/1996/October/originserver_release.html, Myricom Myrinet from Boden, et al., IEEE Micro, Feb., 1995 and http://www.myri.com, and the rest from Figure 7.19, Page 591, Computer Architecture: A Quantitative Approach, by Hennessy and Patterson.

I/O bus references: 32-bit/20-MHz SBus from “History of SPARC systems:- the first decade 1987-1996” (http://www.sparcproductdirectory.com/history.html), 64-bit/66-MHz PCI from “New Ultra 30 workstations signal end of SBus” (http://www.sun.com/sunworldonline/swol-07-1997/swol-07-ultra30.html), and rest from “Peripheral Component Interconnect (PCI) Bus for ASIC Designers” by Howard M. Needham (http://www.ti.com/sc/docs/asic/srga013/toc.htm).