Computer Architecture Screening Exam

Spring 1988

Directions

For the **Breadth** exam, answer questions (1), (2), (3), (4) and (5).
For the **Depth** exam, answer all 8 questions.

(1) A "stack" is an excellent structure that allows for the easy implementation of procedure calls as well as easy expression evaluation. Furthermore, since instructions to manipulate stack operands generally have implicit operands, they are much smaller than instructions that have explicit operands. Because of these reasons, one would expect a proliferation of stack-oriented computers. However, one rarely sees stack-oriented computers any more. Why is this so?

(2) The memory system for a processor has the following characteristics:

(a) A single 4G-byte virtual address space of aligned four-byte words, addressed with 32-bit byte-addresses. The memory system, therefore, accepts the 32-bit addresses, discards the two low-order bits, and uses the upper 30 bits to select one of 2^{30} words.

(b) Pages and page frames are 4K bytes large.

(c) Physical memory will not exceed 2^{26} bytes.

(d) The cache size is 16K bytes, associativity is four-way, block size is 32 bytes, and blocks are tagged with physical addresses.

(e) The Translation Lookaside Buffer (TLB) holds 128 entries and is direct mapped.

Draw a block diagram of the important datapath components and connections for data read or instruction fetch that hits in a cache accessed in parallel with the TLB. Be sure to indicate the width of connections (e.g., how many bits are used to select the set of a reference?). Explicitly state any assumptions you make.

Discuss the advantages and disadvantages of reducing cache associativity to two-way.

(3) A new computer is being designed that will have a very large memory, requiring 40 bits of addressing. It is proposed that a 40-bit address be generated by adding together two 32-bit registers shifted with respect to each other by 8 bits. Thus, a 40-bit address is generated by adding a 32-bit offset to what is effectively a 40-bit segment register. What are the strengths and weaknesses of this approach?

(4) Consider a machine with 16 general purpose registers, 8 addressing modes and a 20 bit wordsize.

(a) You are to design an instruction set format such that there can be 61 2-operand instructions where each of the 2 operands are specified by an addressing mode and a register, 200 2-operand instructions where 1 operand is specified by an addressing mode and a register and the second operand is an absolute address, and 40 no-operand instructions. Notice that you are not given the size of the absolute address field. You must decide on a reasonable choice for the size of this field. In each instruction format specification, label every field, give its width in number of bits, and specify bit values that are critical for differentiating one instruction format from another. You may have to waste some bits, but try to make your format efficient.

(b) Would your instruction format change if the wordsize of the machine doubled to 40 bits? If so, how? If not, why not?

(5)

(a) You are to design a barrel shifter that performs logical right shifts of 8-bit quantities (i.e. zero fill from the left). For this design, you are to use 2-to-1 multiplexors. Thus, your circuit should have 8 input data lines, 8 output data lines and a 3-bit control input. Please be neat when drawing your logical diagram and label it carefully.

(b) Now consider the general case of a barrel shifter that operates on a 2^N-bit datapath. This shifter should peform logical right shifts using 2^M-to-1 multiplexors. As a function of M and N, how many levels of mutliplexors are needed in this barrel shifter? Also as a function of M and N, what is the total number of multiplexors that are needed?

(6) You are designing a high-performance computer that is targeted towards numeric processing. In numeric processing, most of the data structures are large arrays and most programs operate uniformly on array elements. How would this fact influence your choice of the number of registers in your machine? Discuss your choice with respect to instruction set design, relative memory speed, need for a large number of registers, etc.

(7) In a shared memory multiprocessor system, two processes have the following code segments:

```
P1:
    A = 1;
    if (A>B) kill P2;

P2:
    B = 1;
    If (B>A) kill P1;
```

Before these code segments are entered, both A and B are 0. Occasionally, both processes are killed. Explain how this might happen? You may assume that each processor in this system has a local cache and that a cache coherence protocol has been implemented.

(8) It has been argued that the current popularity of so-called Load-Store or Register-to-Register architectures, as opposed to architectures with complex addressing modes, is due to the fact that we are at a "half-way" point in VLSI technology. With today's technology, a high performance CPU fits on a chip only if it is made sufficiently simple. Thus, it is claimed that this current popularity of Load-Store architectures may dwindle as VLSI technology advances.

(i) Argue that, as technology advances, architectures with complex addressing modes will prove to be faster than the Load-Store architectures. In your answer, support general statements with specific explanations or examples of architectural metrics.

(ii) Argue that, as technology advances, Load-Store architectures will continue to provide better performance. Here, too, support your general statementes with specific explanations or examples of architectural metrics.