Computer Architecture Qualifying Breadth Examination

Spring 1989

Directions: Answer all questions.

1. You are trying to design a high-end implementation of an architecture that has a rich set of addressing modes. The addressing modes include autoincrement and autodecrement on any general-purpose regiser, including the program counter. The approach that you want to take is to decode and issue more than one instruction simultaneously. What problems for your high-end implementation might you encounter along the way?

2. Show, using a timing diagram, how a data transfer is carried out between a processor and an arbitrary I/O device. Explain the meaning of, and the need for, all the relevant signals in your timing diagram. What portions are an "overhead" for the actual data transfer? How might this per-transaction overhead be reduced?

3. How does the requirement for allowing unrestricted self-modifying code restrict implementations of high-performance computers? In particular, what is the problem if a computer has no cache memory? Suggest at least one method for dealing with this problem.

4. Many computers use *interleaved* memory. Describe what this means and give an illustrated example. How does interleaving affect memory system throughput and latency? Discuss what factors affect which bits an implementor should select for interleaving.

5. What is a register? What is a cache? What are the principal similarities between registers and caches? What are the prinicpal differences?